What is claimed is:

1. A method of simulating a node, comprising:

forcing an initial logic state on the node;

releasing the node if a predetermined condition is met and creating therefrom a released node;

monitoring the released node; and

providing an indication when the released node is in a preselected condition.

2. The method of claim 1, wherein forcing the initial logic state includes forcing to a logic zero, logic one or high-impedance.

3. The method of claim 1, wherein releasing the node further comprises determining that the condition is met after passage of a predetermined amount of time.

4. The method of claim 3, wherein releasing the node further comprises determining that the condition is met when the node has been resolved

5. The method of claim 1, wherein providing an indication includes indicating when the released node is in an unknown logic state.

6. The method of claim 1, further comprising providing an error indication when the released node is a preselected condition.

7. The method of claim 3, further comprising selecting a user-defined time period for the predetermined amount of time.

8. A method of initializing and monitoring a simulated circuit node, comprising:

obtaining an initial node condition for a node;

forcing the node to the initial node condition;

simulating a circuit containing the node;

testing the node for a valid condition;

monitoring the node; and

providing an indication when the node is in an undesirable condition.

9. The method of claim 8, wherein the initial node condition is forced again if the testing results in the node resolving to an unknown logic value.

10. The method of claim 9, wherein the initial node condition is forced and simulation is repeated until the node resolves to a valid logic value.

11. The method of claim 10, wherein monitoring only occurs after the node resolves to a valid logic value.

12. The method of claim 8, further comprising outputting the condition of the simulated node.

13. The method of claim 8, further comprising obtaining a simulation run time.

14. The method of claim 13, further comprising outputting a final node condition when the simulation run time is completed.

15. A computer-readable medium having computer-executable instructions comprising:

forcing an initial logic state on the node;

releasing the node if a predetermined condition is met and creating therefrom a released node;

monitoring the released node; and

providing an indication when the released node is in a preselected condition.

16. The medium of claim 15, having further computer-executable instructions for forcing the initial logic state to a logic zero, logic one or high-impedance.

17. The medium of claim 15, having further computer-executable instructions for determining that the condition is met after passage of a predetermined amount of time.

18. The medium of claim 15, having further computer-executable instructions for determining that the condition is met when the node has been resolved

19. The medium of claim 8, having further computer-executable instructions for indicating when the released node is in an unknown logic state.

20. A simulation module for initializing and monitoring a simulated circuit node, comprising:

an input means for inputting an initial node condition;

a conveying means for conveying the initial node condition to a simulated node;

release means for releasing the node upon satisfaction of a condition;

a monitoring means for monitoring the simulated node for a node condition; and

an output means for outputting an indication when the node condition is in an undesirable state.

21. The module of claim 20, further comprising an output means for outputting the node condition.

22. The module of claim 20, further comprising an input means for inputting a simulation run time.

23. The module of claim 22, further comprising an output means for outputting a final node condition at completion of the simulation run time.

24. A computerized system for initializing and monitoring a simulated circuit node, the system comprising:

a circuit simulation tool;

a first input module inputting an initial node condition;

a conveying module conveying the initial node condition to a simulated node;

a release module releasing the initial condition;

a monitoring module monitoring the simulated node for a node condition;

a first output module outputting an indication when the node condition is in an undesirable state;

a second input module inputting a simulation run time; and

a second output module outputting a final node condition at completion of the simulation run time.

25. An HDL initial condition module comprising a means for maintaining a logic level of a simulated circuit node until a release condition is met.

26. The module of claim 25 wherein the release condition is when the node can be resolved to a known logic state.

27. The module of claim 25 wherein the logic level is a value defined by an HDL executable simulation program.

28. An HDL initial condition module having an initial condition release means and a simulated circuit node error detection means.

29. An HDL initial condition module comprising means for maintaining a logic level of a simulated circuit node for a predetermined period of time, means for releasing an initial condition, and wherein the predetermined period of time is a simulation run time defined by an HDL simulation executable program.

30. The module of claim 29, wherein the predetermined period of time is a user-defined period of time.

31. An HDL simulated circuit device, comprising:

a first HDL module comprising:

a first input submodule inputting a first initial node condition;

a first conveyance submodule conveying the first initial node condition to a first simulated node;

a first monitor submodule monitoring the first simulated node for a first node condition; and

a first output submodule outputting a first indication when the first node condition is in an undesirable state;

a second HDL module comprising:

a second input submodule inputting a second initial node condition;

a second conveyance submodule conveying the second initial node condition to a second simulated node;

a release submodule releasing the node on a predetermined condition;

a second monitor submodule monitoring the second simulated node for a second node condition; and

a second output submodule outputting a second indication when the second node condition is in an undesirable state; and

wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule.

32. An HDL simulated circuit device, comprising:

a first HDL module comprising:

a first input;

a first conveyance;

a first node condition output

a second HDL module comprising:

a second input;

a second conveyance;

a third HDL module comprising:

a release condition;

wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid.

33. An HDL design tool, comprising:

a circuit simulation device; and

a plurality of selectable modules capable of being linked to the circuit simulation device, wherein at least one of the selectable modules executes the following commands:

inputting an initial node condition;

conveying the initial node condition to a simulated node;

releasing the node if a condition is met;

monitoring the simulated node for a node condition; and

an output means for outputting an indication when the node condition is in an undesirable state.

34. A simulation method, comprising:

phase one, including;

forcing an initial logic zero, logic one or high-impedance on a node;

releasing the node;

testing to see if the node has been resolved;

if the node has been resolved, continue to phase two

if the node has not been resolved, continuing in phase one

phase two, including;

monitoring the node value;

testing the node value;

indicating an error if an unacceptable condition appears on the node;

and,

continuing in phase two until simulation completion.

35. The method of claim 34, wherein simulation completion is a user defined time period.